

CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

High-Voltage Types (20-Volt Rating)

■ CD4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

Applications:

- Parallel Input/Parallel Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

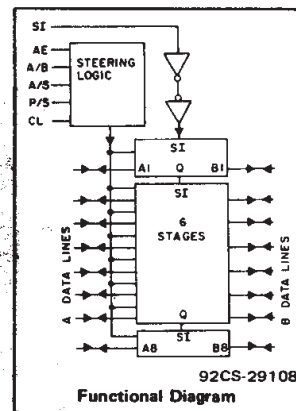
The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034B packages.

The CD4034B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal)	–0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –55°C to +100°C	500mW
For T_A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	–55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C



Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines (3-state output)
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation dc-to-10 MHz (typ.) at V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

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RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S				
	Serial Data to Clock	5	160	—
		10	60	—
		15	40	—
	Parallel Data to Clock	5	50	—
		10	30	—
Clock Pulse Width, t_W				
		5	350	—
		10	140	—
Clock Input Frequency, f_{CL}				
		5	2	MHz
		10	5	MHz
Clock Input Rise or Fall Time, t_{rCL} , t_{fCL} *				
		15	7	MHz
Clock Input Rise or Fall Time, t_{rCL} , t_{fCL} *	5, 10, 15	—	15	μs

*If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

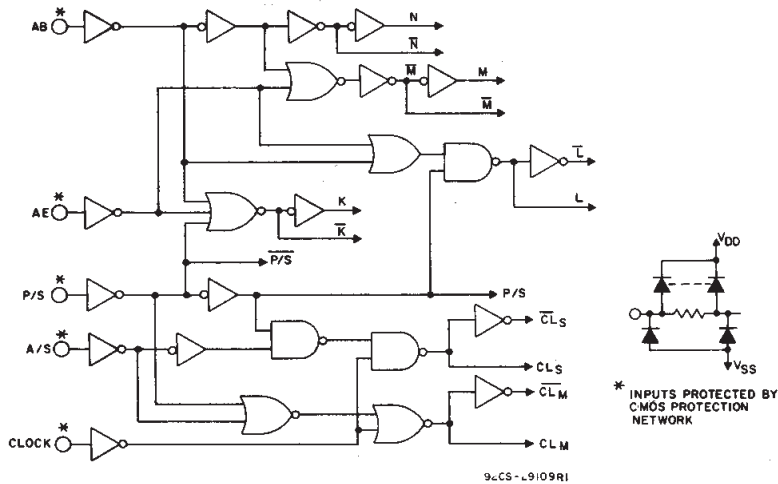


Fig. 1 — Steering logic diagram.

FLIP-FLOP TRUTH TABLE

INPUTS			OUTPUT
$\overline{CLM}$	$\overline{CLS}$	D	Q
Low	Low	0	0
High	Low	0	0
Low	High	0	INVALID CONDITION
High	High	X	0
Low	Low	1	1
High	Low	1	1
Low	High	1	INVALID CONDITION

1 = High Level 0 = Low Level X = Don't Care

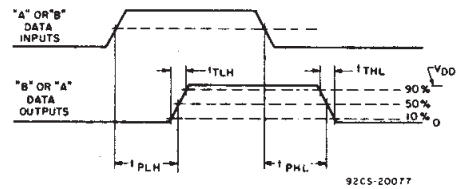
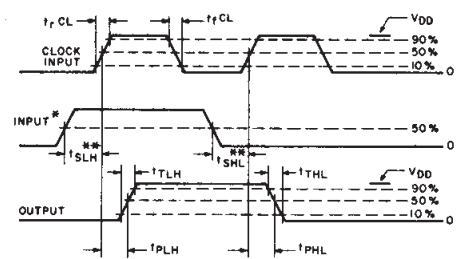


Fig. 2 — Asynchronous operation propagation delay time and transition time.



* INPUT REFERS TO ANY OF THE "A" OR "B" DATA INPUTS, "A" ENABLE, SERIAL INPUT, A/B, P/S, OR A/S INPUTS

** t_{SLH} AND t_{SHL} ARE SET-UP TIMES

92CS-20078

Fig. 3 — Synchronous operation propagation delay times, transition times, and set-up times.

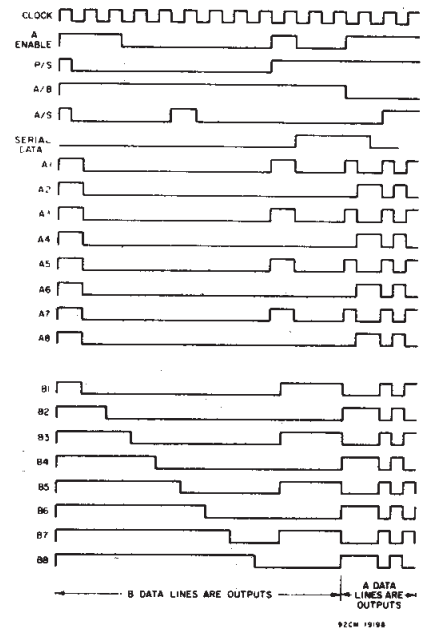


Fig. 4 — Timing diagram.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current* I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
3-State Output Leakage Current I _{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 ⁻⁴	±0.4	μA

* All inputs except A and B Lines.

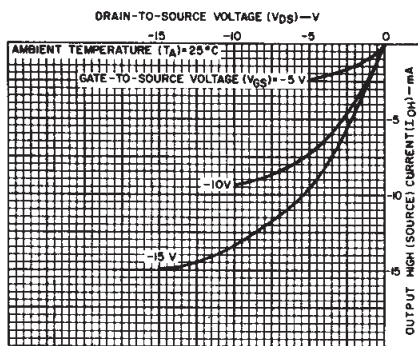


Fig. 8 — Minimum output high (source) current characteristics.

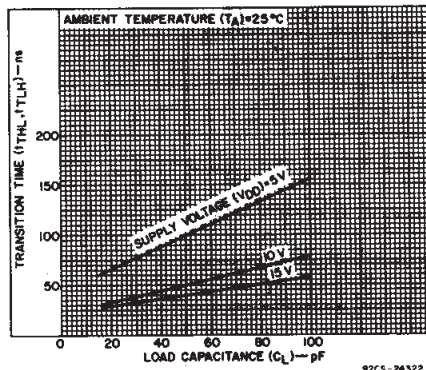


Fig. 9 — Typical transition time as a function of load capacitance.

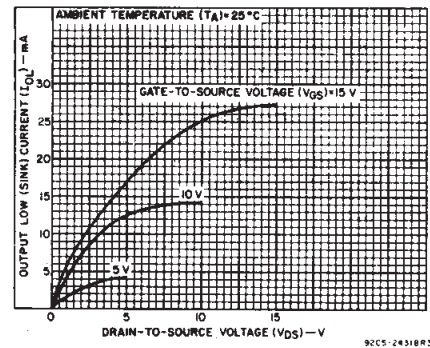


Fig. 5 — Typical output low (sink) current characteristics.

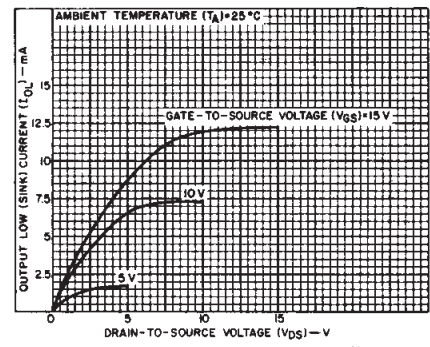


Fig. 6 — Minimum output low (sink) current characteristics.

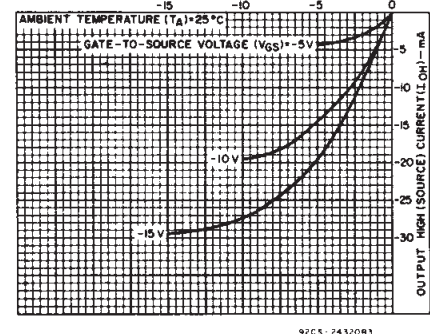


Fig. 7 — Typical output high (source) current characteristics.

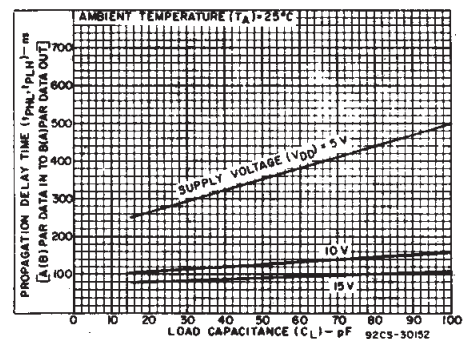


Fig. 10 — Typical propagation delay time as a function of load capacitance [A(B) parallel Data Input to B(A) parallel Data Output, synchronous or asynchronous].

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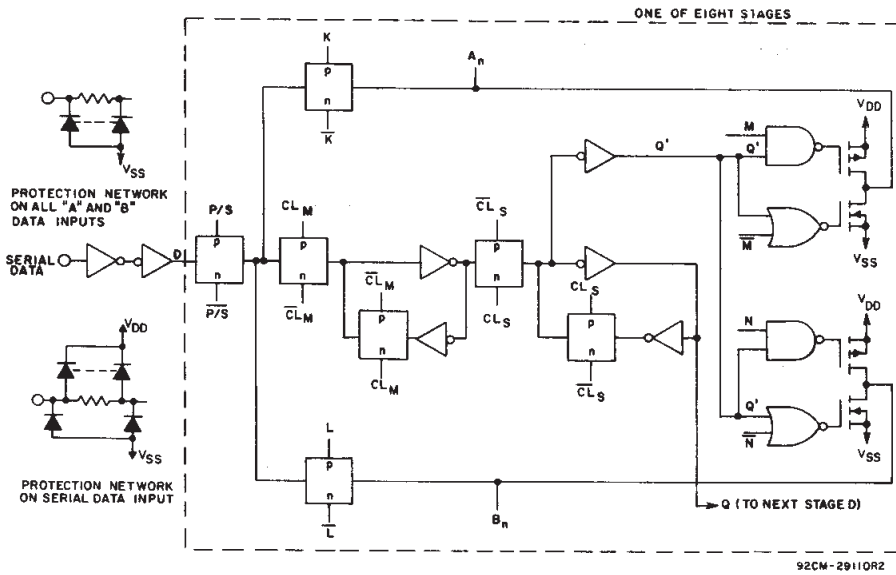


Fig. 11 - Register stage logic diagram (1 of 8 stages).

TRUTH TABLE FOR REGISTER INPUT-LEVELS AND
RESULTING REGISTER OPERATION

"A" Enable	P/S	A/B	A/S	Operation*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode. During transfer from parallel to serial operation A/S should remain low in order to prevent D_S transfer into Flip Flops.

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

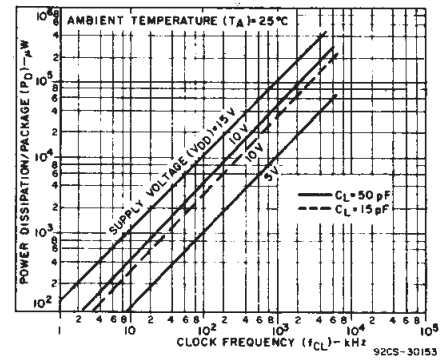


Fig. 12 - Typical dynamic power dissipation as a function of clock frequency.

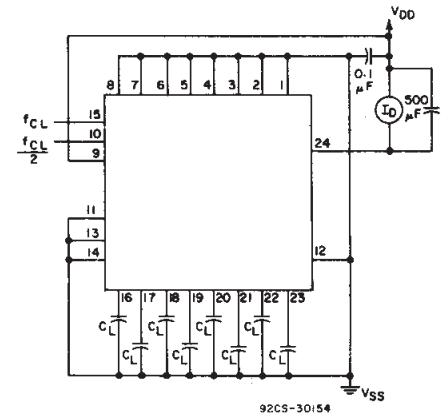


Fig. 13 - Dynamic power dissipation test circuit.

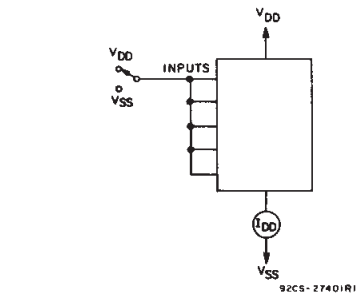


Fig. 14 - Quiescent device current test circuit.

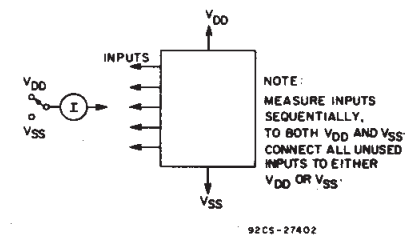


Fig. 15 - Input current test circuit.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_i, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	—	350	700	ns
A(B) Parallel Data In to	10	—	120	240	
B(A) Parallel Data Out	15	—	85	170	
Serial to Parallel Data Out					
3-State Propagation Delay t_{PLZ}, t_{PHZ}	5	—	200	400	
A/B or AE to "A" OUT t_{PZL}, t_{PZH}	10	—	80	160	
	15	—	60	120	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Data Setup Time, t_{SU}	5	—	80	160	ns
Serial Data to Clock	10	—	30	60	
	15	—	20	40	
Parallel Data to Clock	5	—	25	50	
	10	—	15	30	
	15	—	10	20	
Minimum Data Hold Time, t_H	5	—	—	50	ns
	10	—	—	15	
	15	—	—	10	
Minimum High-Level Pulse Width, t_W	5	—	175	350	
AE, P/S, A/S	10	—	70	140	
	15	—	40	80	
Maximum Clock Frequency, f_{CL}	5	2	4	—	MHz
	10	5	10	—	
	15	7	14	—	
Minimum Clock Pulse Width, t_W	5	—	125	250	ns
	10	—	50	100	
	15	—	35	70	
Maximum Clock Rise or Fall Time, t_{CL}, t_{CL}^*	5,10,15	—	—	15	μs
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

*If more than one unit is cascaded t_{CL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

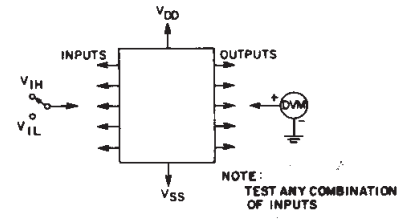


Fig. 16 - Input-voltage test circuit.

Applications

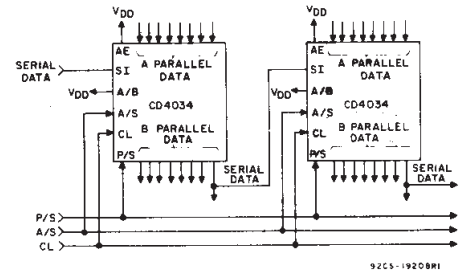


Fig. 17 - 16-bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

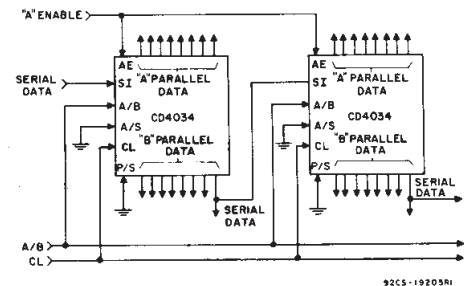
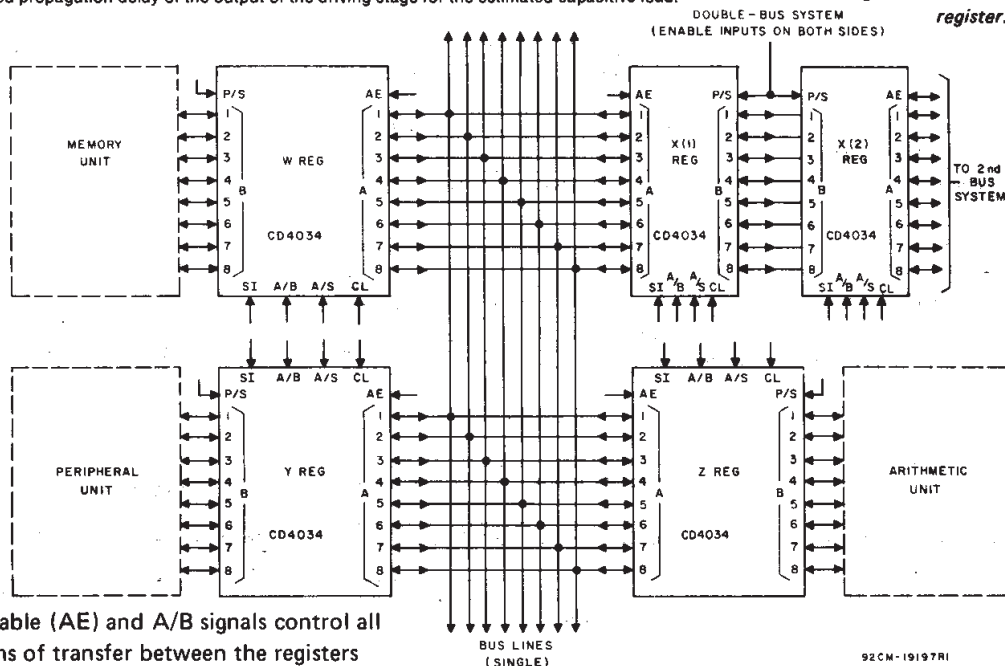


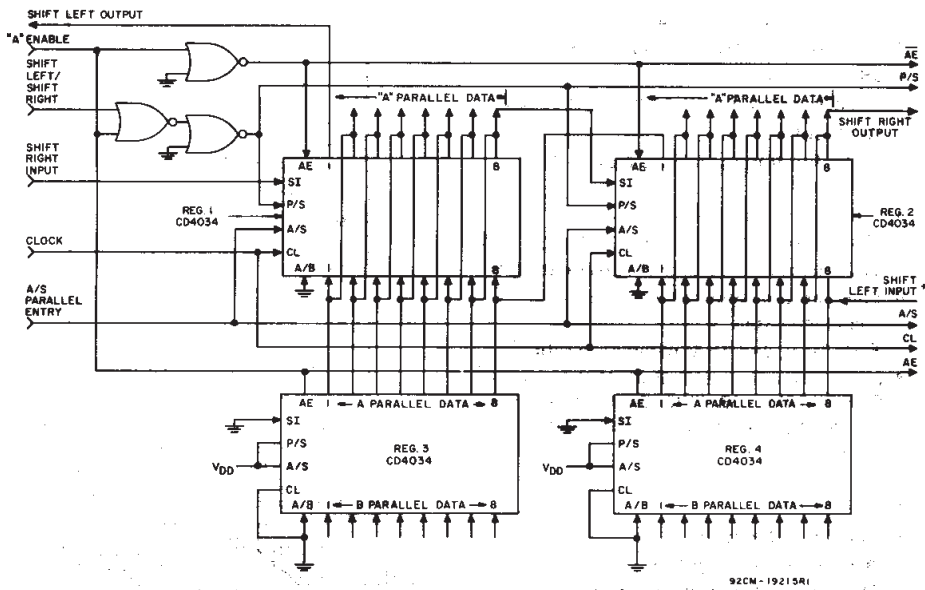
Fig. 18 - 16-bit serial in/gated parallel out register.



The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems.

Fig. 19 - Single- and double-bus systems.

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A "High" ("Low") on the shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data

into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

* Shift left input must be disabled during parallel entry.

Fig. 20 - Shift right/shift left with parallel inputs.

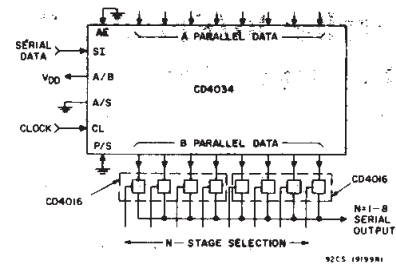


Fig. 21 - N-stage shift register with fixed serial output line.

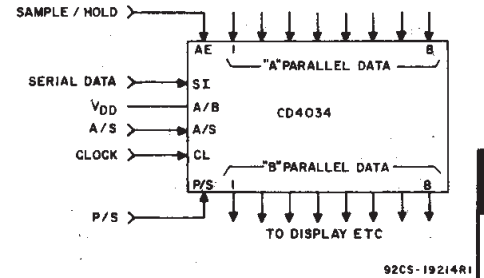
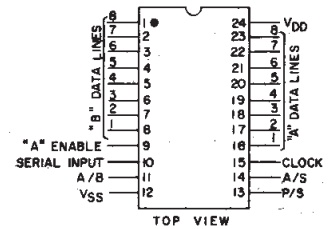
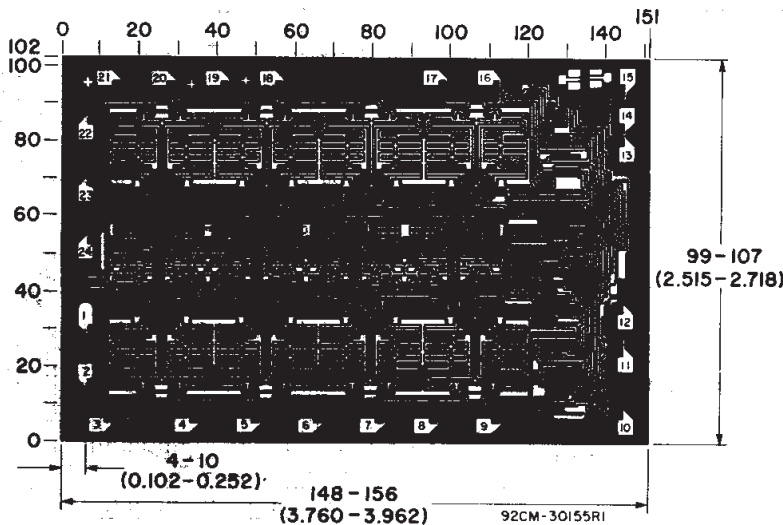


Fig. 22 - Sample and hold register-serial/parallel in-parallel out.



TERMINAL DIAGRAM

92CS-20744R1



Dimensions and pad layout for CD4034BH.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4034BE	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4034BEE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4034BF3A	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
CD4034BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4034BM96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4034BM96E4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4034BM96G4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4034BME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4034BMG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4034BNSR	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
CD4034BNSRE4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
CD4034BNSRG4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
CD4034BPW	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
CD4034BPWE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
CD4034BPWG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
CD4034BPWR	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
CD4034BPWRE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
CD4034BPWRG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4034BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

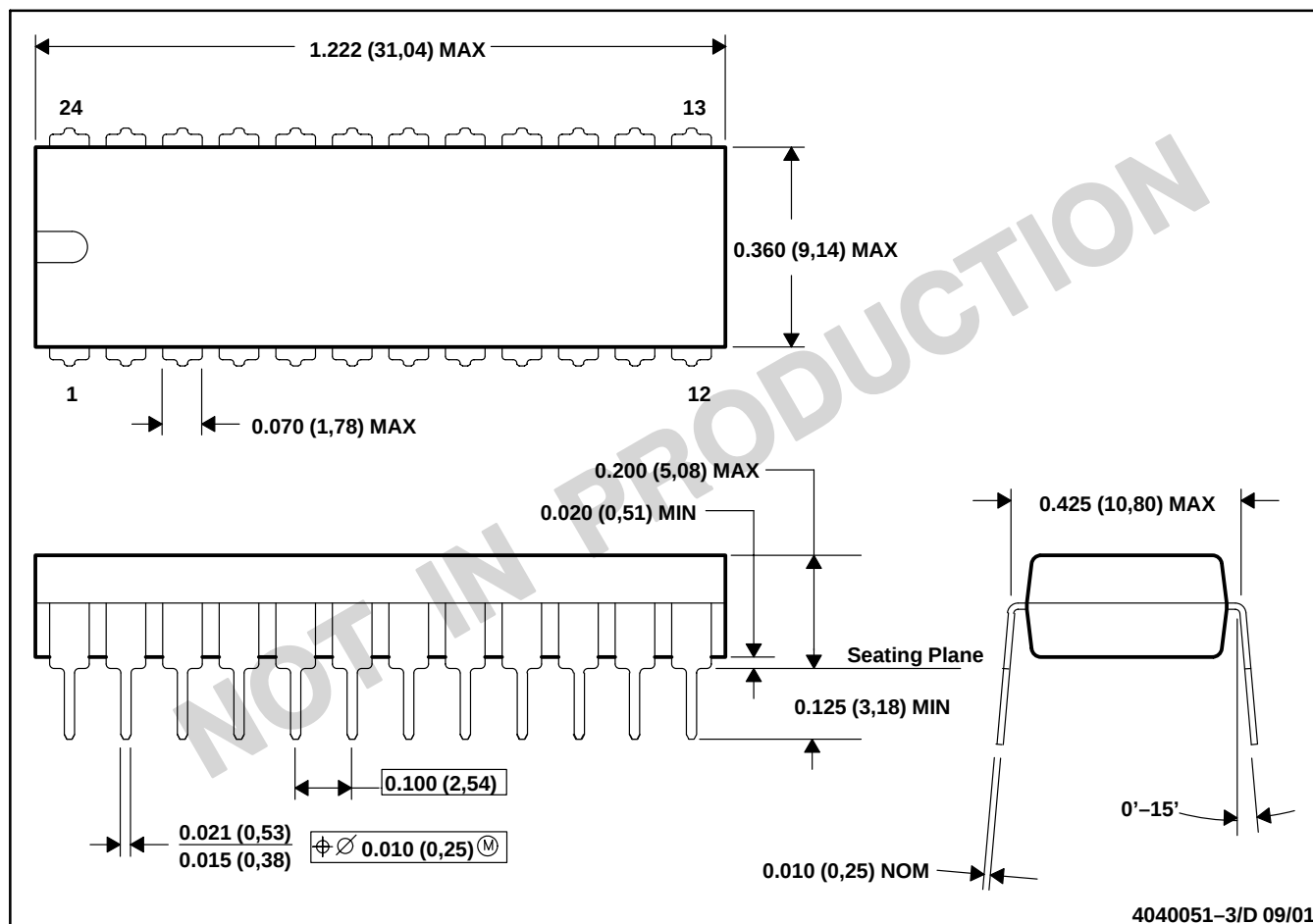


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4034BM96	SOIC	DW	24	2000	346.0	346.0	41.0

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-010

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

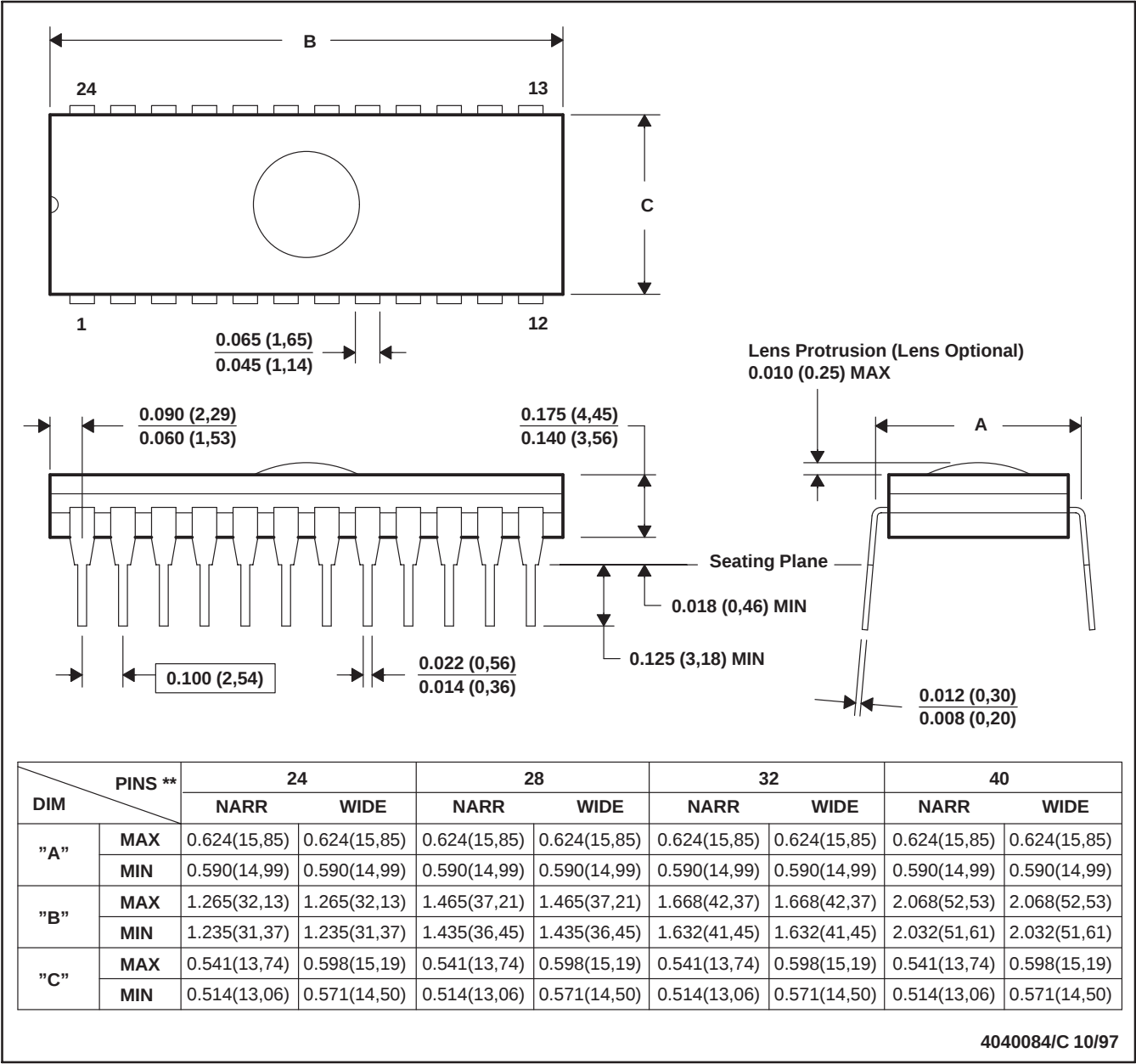
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

J (R-GDIP-T**)
24 PINS SHOWN

CERAMIC DUAL-IN-LINE PACKAGE

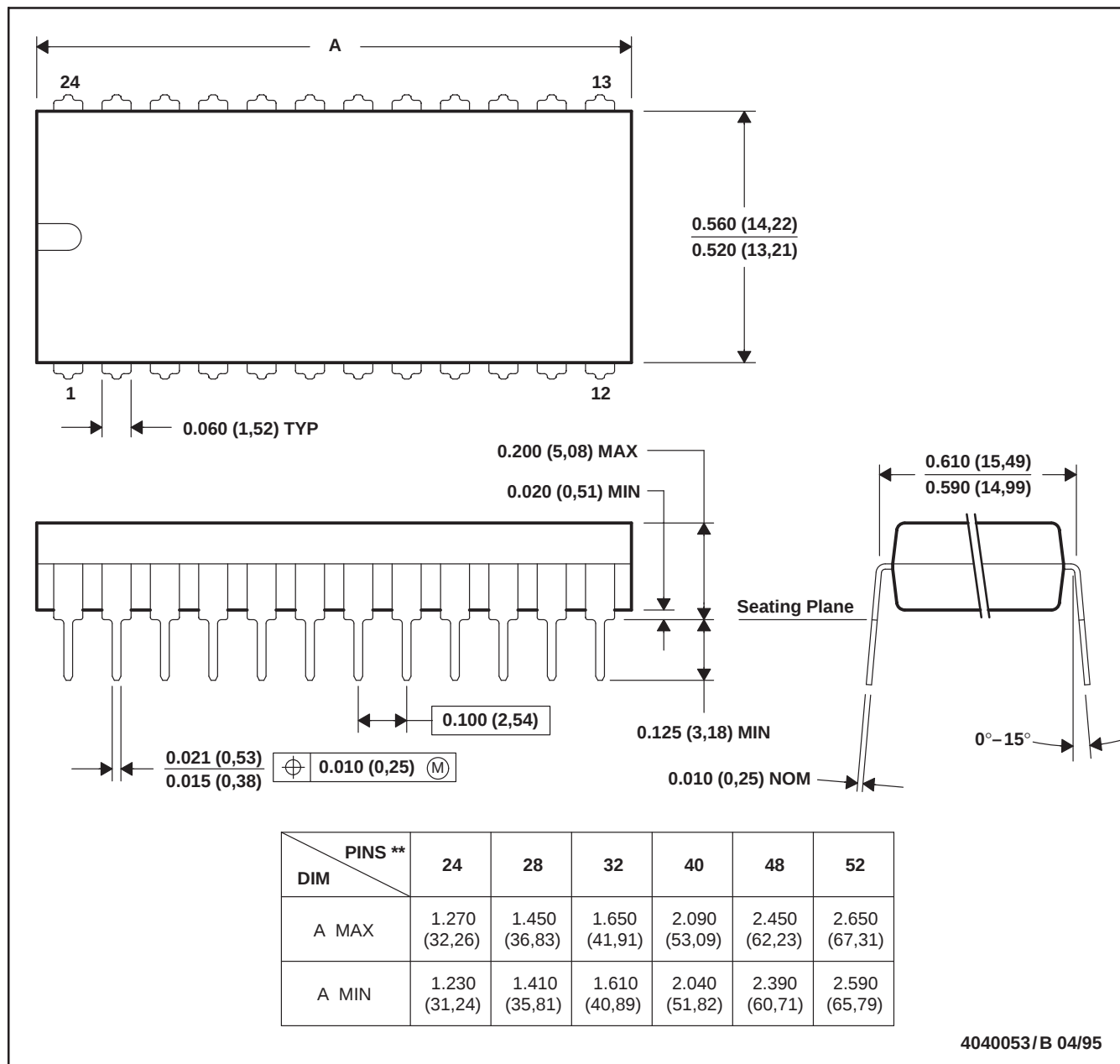


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

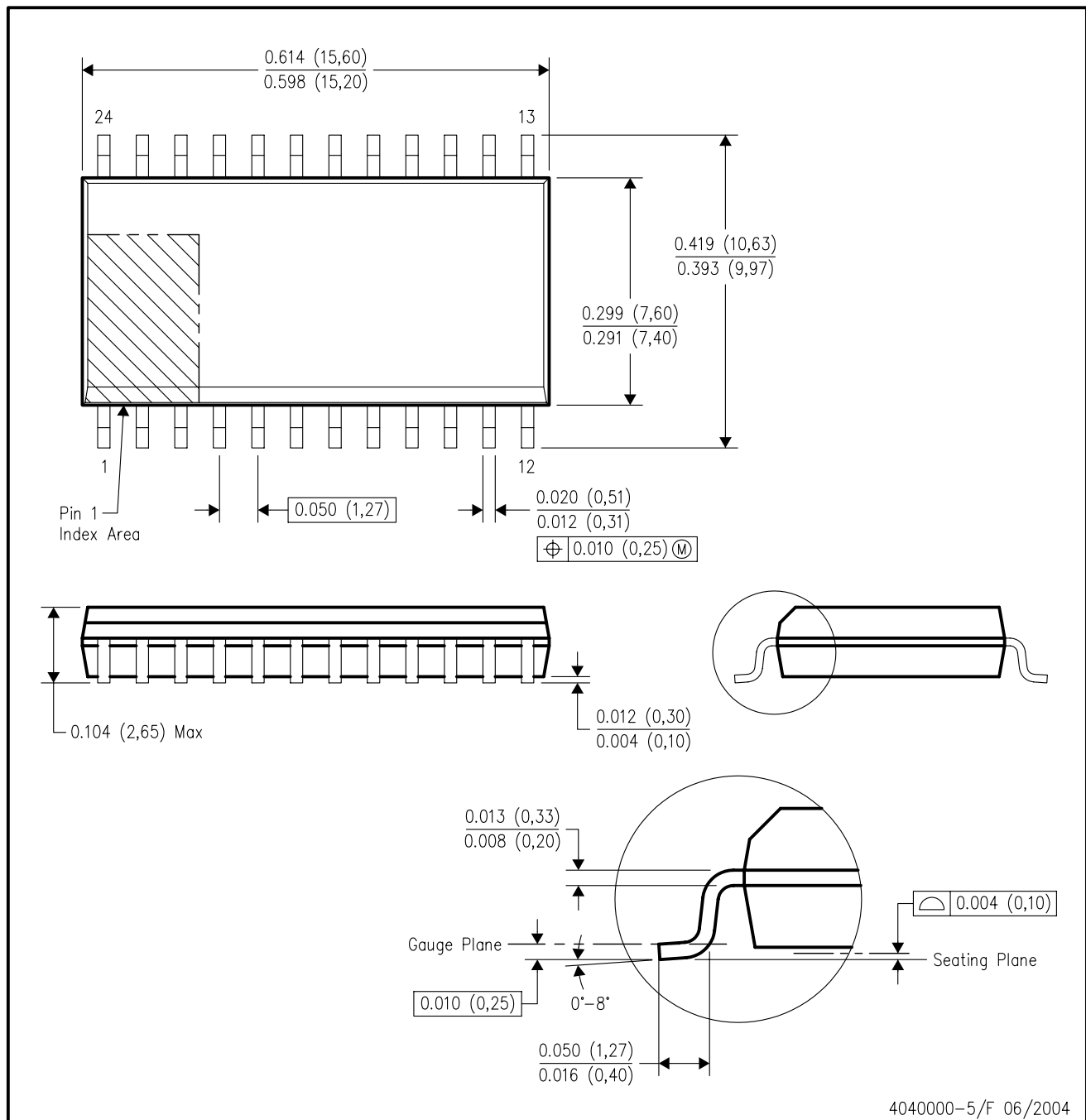
24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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